# CDCM7005 (QFN Package) Evaluation Module Manual

## HPA/High Speed Communications

# User's Guide

2005

Clock Drivers

SCAU015

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## Preface

# Read This First

### *About This Manual*

This manual explains how to use the CDCM7005 evaluation module (EVM) and provides guidelines to build the customer's own systems. The manual includes schematics, layout, bill of materials, and a software description.

### *How to Use This Manual*

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Quick Start
- Chapter 3—EVM Hardware
- Chapter 4—Serial Peripheral Interface (SPI) Software
- Chapter 5—Schematics, Board Layout, and Parts List

### *Related Documentation From Texas Instruments*

- CDCM7005 Data Sheet, SCAS793, Texas Instruments

### *FCC Warning*

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### *If You Need Assistance. . .*

If you need assitance with this device, please email
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Chapter 1

# Introduction

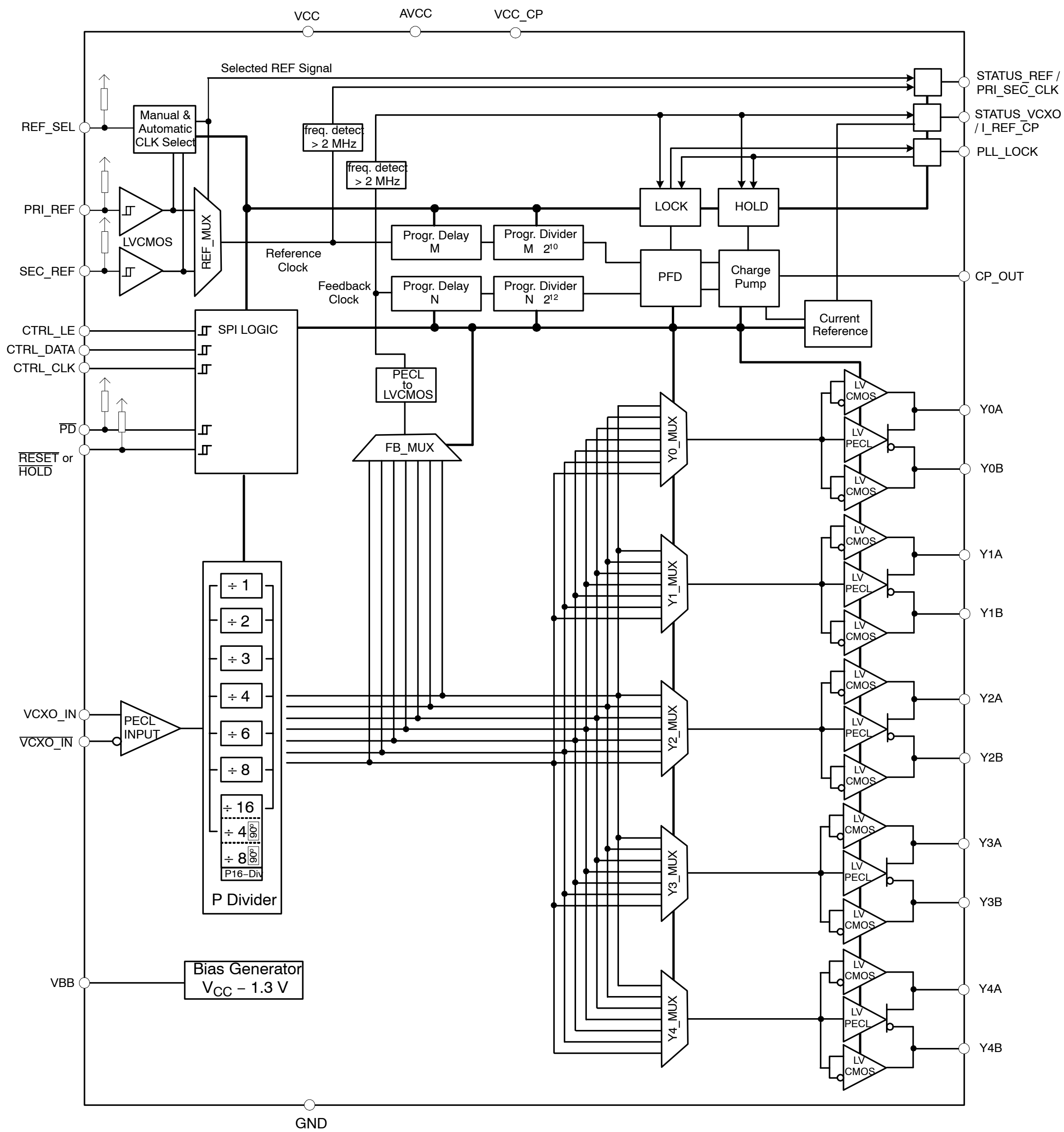
The CDCM7005 is a high-performance, low phase noise and low skew clock synchronizer that synchronizes an on-board voltage controlled crystal oscillator (VC(X)O) frequency to an external reference clock. The device operates up to 2.2 GHz. The PLL loop bandwidth and damping factor can be adjusted to meet different system requirements by selecting the external VC(X)O, loop filter components, frequency for PFD, and charge pump current. Each of the five differential LVPECL and five LVCMOS pair outputs can be programmed by a serial peripheral interface (SPI). The SPI allows individual control of the frequency and enable/disable state of each output. As the system requires external components like a loop filter and VC(X)O, this EVM provides an easy method to evaluate and modify the performance and parameters of the clock system in conjunction with the specific customer application. Loop bandwidth can be selected as low as 10 Hz or less, allowing the device to clean the system's clock jitter.

In non PLL mode, the CDCM7005 can be used as a simple LVPECL or LVCMOS buffer with divider options.

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**1.1 CDCM7005 Functional Block Diagram .......................... 1-2**

## 1.1 CDCM7005 Functional Block Diagram



Chapter 2

# Quick Start

In order to setup the EVM quickly and to take some measurements at default settings, the following actions are required:

- ❑ Supply 3.3 V to P1, LED D4 will be on.
- ❑ Apply a single-ended reference clock to the reference clock input PRI_REF (pin A1) or SEC_REF (pin B1). For default setting, the reference clock must be $1/8^{th}$ of the VC(X)O frequency. If REF_SEL is set to 1, then PRI_REF is selected. If REF_SEL is set to 0, then SEC_REF is selected. This selection can be realized via J26 (header 1 and 2 is high; header 2 and 3 is low).
- ❑ Connect Y0/Y0B (or Y1/Y1B) to oscilloscope in order to check an output signal. Ensure the oscilloscope has 50 Ω to ground termination.

After power up, D1 is on if there is a valid reference clock and D2 is on if there is a valid VC(X)O clock for the CDCM7005. If D3 turns on, then the reference clock and the VC(X)O clocks are phase locked.

Chapter 3

# EVM Hardware

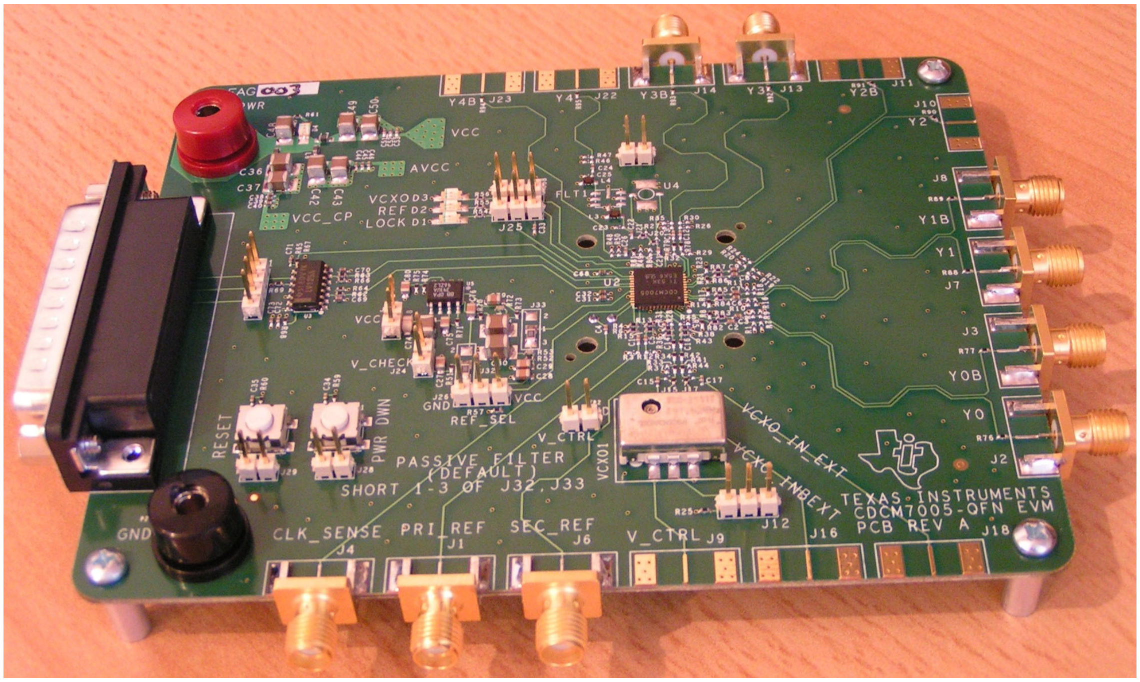
This chapter discusses the EVM hardware.

**Topic** **Page**


3.1 Board View and Connector Location . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 3-2
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## 3.1 Board View and Connector Location

*Figure 3−1. Board View*




## 3.2 Hardware Configuration

This section describes the board configuration using on-board jumpers and solder bridges.

### 3.2.1 Power Supply (P1, P2)

- Supply 3.3 V ±10% on P1 and P2 using a stabilized external power supply.
  - **WARNING: Never supply more than 3.6 V on P1.**

### 3.2.2 Onboard Switches and Indicators (SW1−SW2, D1−D4)

- Push SW1 to enter the power-down mode of the CDCM7005 device. Then all current sources are switched off, all outputs are switched into 3-state, and all dividers (M, N, and P) are reset to default.
- Push SW2 to enter the reset mode of the device. The charge pump (CP) is switched to 3-state and all counters (N, M, P) are rest to zero (the initial divider settings are maintained in SPI.
- The three status outputs of the CDCM7005 are fed to LED indicators. D1 on indicates a valid reference input clock signal. D2 is on if the VC(X)O input clock is valid and D3 turns on if the PLL has been locked.
- D4 indicates power supply

**Note:**

In case of a low input impedance of the VC(X)O control voltage input, there is a possibility D3 may not turn on to indicate locking.

### 3.2.3 Programming Interfaces (J30, J31)

The SPI of the device is used for writing to the control register of the device. It consists of three control lines CTRL_CLK, CTRL_DATA, and CTRL_LE. There are four 30-bit wide RAM registers, which can be addressed by the two LSBs of a transferred word. Every transmitted word must have 32 bits, starting with MSB. After supplying power or activating the power-down mode, the registers are loaded with the device default values internally (see the CDCM7005 data sheet, SCAS793). However, if specific register settings are required for any applications, there are two ways to program the device externally:

❑ Connect the parallel port cable to the PC and EVM parallel port. This needs control S/W (see Chapter 4).

### 3.2.4 Loop Filter (J32−J34)

The loop filter is one of the key elements determining the loop bandwidth of the PLL. The loop filter converts the charge pump current into the control voltage for the voltage controlled oscillator. The phase difference between the input clocks of the phase frequency detector determines the width of the charge pump output current pulses. These high frequency pulses are transformed into a voltage to control the oscillator.

Basically, three types of loop filters are implemented on the EVM.

❑ Passive loop filter

❑ External active loop filter using an external low-noise OPA.

Filter types can be selected by soldering bridges J32−J34, see Table 3−1. Control voltage of the VC(X)O can be measured at J9 or TP1. If an external OPA is used, it needs to be switched on by connecting J34. For example, passive filter operation is provided when pads 1 and 3 of J33 are solder bridged and pads 1 and 3 of J32 are solder bridged.

*Default setting: Passive Loop Filter*

*Table 3−1. Filter Configurations*

| Bridge | Passive Filter | Active With An External OPA |
|---|---|---|
| J33 | 1−3 | 1−2 |
| J34 | Open | Closed |
| J32 | 1−3 | 1−2 |

### 3.2.5 High-Speed Outputs and Inputs (J1−J4, J6−J11, J13, J14, J22, and J23)

The CDCM7005 drives five differential LVPECL outputs. All PECL outputs are ac-coupled and terminated with 150 Ω to GND. This is in contrast to typical LVPECL termination, which requires $V_{CC}$ − 2 V as termination voltage. The reason is to simplify the power supply scheme. The device output's trace impedance is 50 Ω and traces are matched in length. All outputs have options for pullup and pulldown resistors.

When the CDCM7005 is powered up, it defaults to five LVPECL outputs. However, this EVM is configured as follows:

- ❑ Y0 – Y2 = LVPECL
- ❑ Y3, Y4 = LVCMOS (in addition Y4 has an option for a custom filter)

The reference input clock signal has to be applied to J1 or J6. The reference input clock signal can be sensed on J4. In this case, close the bridge J5 (the oscilloscope's 50 Ω may be used to terminate the 50-Ω trace). The reference input clock sense line is matched to the LVPECL outputs line to avoid any additional delay offset. The input is ac-coupled (C4).

### 3.2.6 VC(X)O Inputs and Outputs (J16–J18)

The CDCM7005 requires an external VC(X)O in order to complete the PLL loop. The VC(X)O adjusts the frequency and phase depending on the control voltage level coming from the loop filter and provide the input clock to the LVPECL block.

Another option would be to use an external source via J16 and J18.

### 3.2.7 AC-Coupling at PRI_REF (C1, R4, R6) and SEC_REF (C5, R13, R15)

An ac-coupling is provided at PRI_REF and SEC_REF to ease the use of the CDCM7005 with different signaling levels (LVCMOS, LVPECL, LVDS,...). However, the ac-coupling will increase the PLL stabilization time after power up due to transient effects. It also increases the switching time between PRI_REF and SEC_REF in case of automatic reference clock switching. Therefore, the ac-coupling must be removed for optimized system performance (C1 and C5 has to be replaced with an 0-Ω resistor and R4, R6, R13, and R15 have to be removed).

Chapter 4

# Serial Peripheral Interface (SPI) Software

This chapter discusses the serial peripheral interface software.

**Topic** **Page**


**4.1 Functional Description . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 4-2**
**4.2 Software Installation . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 4-2**

## 4.1 Functional Description

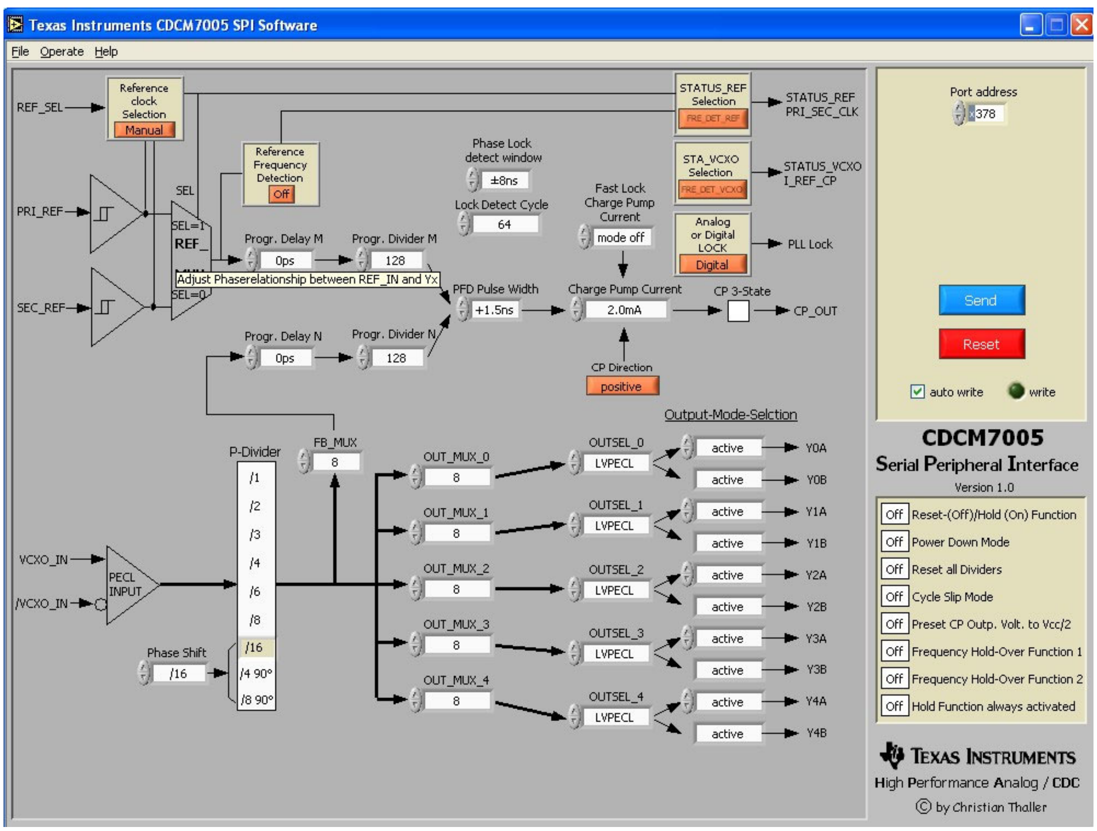
Programming software here as described is intended for programming the internal control register of the CDCM7005. The software runs under Windows98, NT, 2000, and XP. A quick installation is required prior to use. See the *Software Installation* section.

There are several cases where programming is mandatory.

As a rule of thumb here are some examples:

- ❑ Use of active loop filter
- ❑ Change of divider ratio or disable of certain LVPECL/LVCMOS outputs
- ❑ Select between LVPECL or LVCMOS output
- ❑ Change of phase offset, (Delay M/N), or selection of 90’ or 180’ phase shift
- ❑ Change of charge pump output current.
- ❑ Widening the lock detect window

*Figure 4−1. Screen View*




## 4.2 Software Installation

Follow the steps below in order to install the SPI control software:

1) Run program setup.exe in the Installer folder
2) Reboot your computer
3) Run the Software from Start –> Programs –> CDCM7005_EVM –> CDCM7005_EVM

Chapter 5

# Application Circuit Diagram

This chapter discusses the application circuit diagram.

**Topic** **Page**

**5.1 Application Circuit Diagram . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 5-2**

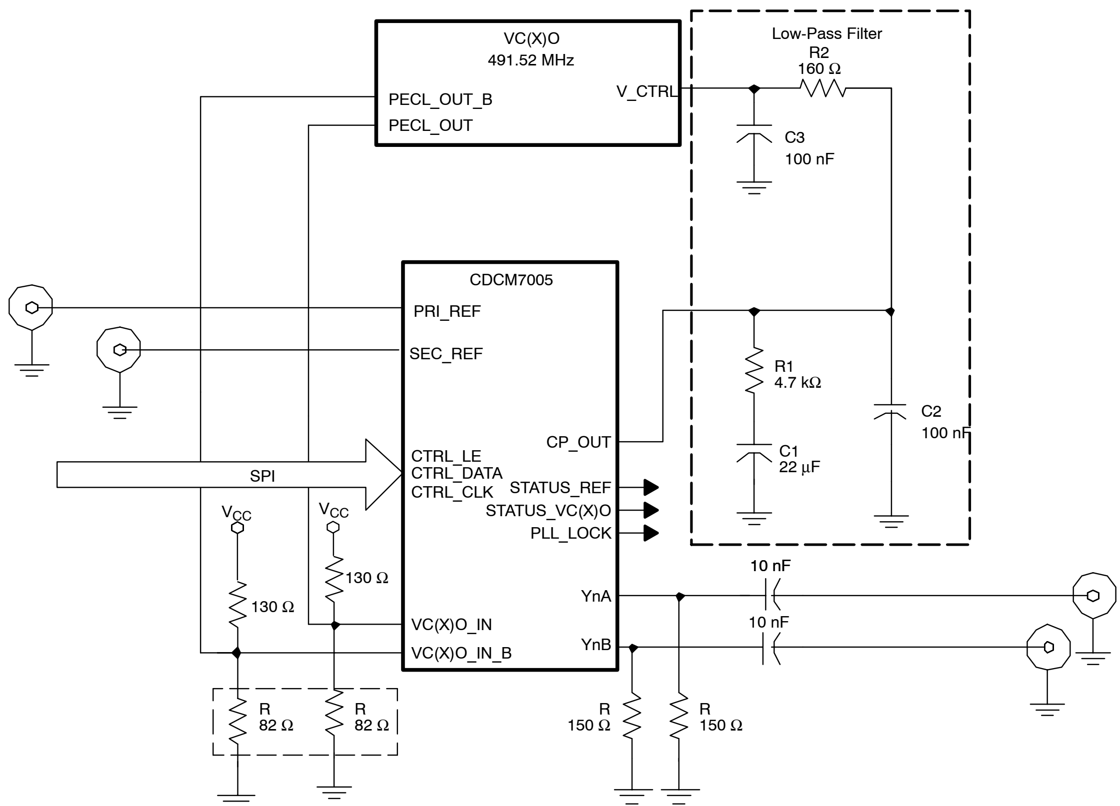
## 5.1 Application Circuit Diagram

The following applications sections the two loop filter configurations are discussed.

### 5.1.1 Passive Loop Filter

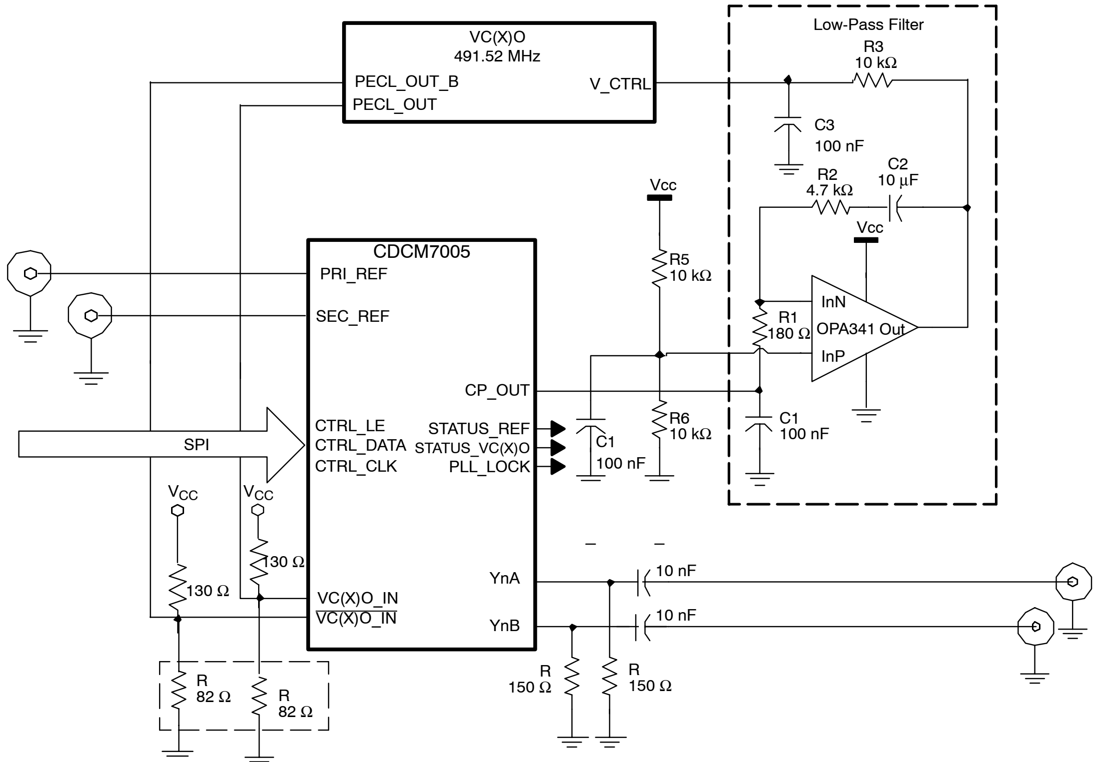
The passive loop filter is a second order filter (two poles, one zero). The zero is required for the overall loop stability. R1, C1, and C2 generate the dominant pole of the system. A second pole is introduced by R2 and C3.

*Figure 5−1. CDCM7005 With a Passive Loop Filter Configuration*



### 5.1.2 External Active Loop Filter Using OPA341

*Figure 5−2. CDCM7005 With a External Active Loop Filter Using OPA341*



Chapter 6

# Parts List, Board Layout, and Schematics

This chapter contains the parts list, board layout, and schematics for the CDCM7005 EVM.

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6.1 Parts List . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6-2

6.2 Board Layout . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6-4

6.3 Schematics . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 6-8

## 6.1 Parts List

| Item | QTY | Reference Designator | Footprint | Part | Part Number |
|---|---|---|---|---|---|
| 1 | 24 | C1−C9, C12, C13, C15, C17, C26, C40, C41, C46, C47, C53, C54, C56−C58, C66 | smd_cap_0402 | 10 nF | Panasonic ECJ−0EB1E103K |
| 2 | 2 | C72, C10 | smd_cap_0402 | 100 nF | Panasonic ECJ−0EB1E104K |
| 3 | 7 | C11, C32, C62−C64, C68, C73 | smd_cap_0402 | 100 pF | Panasonic ECJ−0EB1E101K |
| 4 | 2 | C14, C16 | smd_cap_0402 | 0 Ω | Panasonic ERJ−2GE0R00X |
| 5 | 1 | C18 | smd_cap_0402 | 1000 pF | Panasonic ECJ−0EB1E102K |
| 6 | 1 | C19 | smd_cap_0603 | 1 µF | Panasonic ECJ−1VF1C105Z |
| 7 | 2 | C20, C22 | smd_cap_0402 | 0.1 µF | Panasonic ECJ−0EB1A104K |
| 8 | 1 | C21 | smd_cap_0402 | 10 nF | Panasonic ECJ−0EB1E103K |
| 9 | 1 | C23 | smd_cap_0402 | NU 1.1 pF | NU Rohm MCH155A1R1CK |
| 10 | 1 | C24 | smd_cap_0402 | 22 pF | Panasonic ECJ−0EC1H220J |
| 11 | 1 | C25 | smd_cap_0402 | NU 1 pF | NU Rohm MCH155A1R1CK |
| 12 | 7 | C27−C29, C75, C76, C79, C80 | smd_cap_0805 | 0.1 µF | Panasonic ECP−U1C104MA5 |
| 13 | 1 | C30 | smd_cap_1210 | 22 µF | Murata GRM32ER71A226KE20L |
| 14 | 1 | C31 | smd_cap_0402 | 22 nF | Panasonic ECJ−0EB1E104K |
| 15 | 3 | C33−C35 | smd_cap_0402 | 10 nF | Panasonic ECJ−0EF1H103Z |
| 16 | 4 | C36, C42, C48, C49 | smd_cap_1210_pol | 22 µF | Panasonic ECS−T1CC226R |
| | | C49 | smd_cap_1210_pol | 22 µF | Panasonic ECS−T1CC226R |
| 17 | 5 | C37, C43, C50, C55, C65 | smd_cap_1210_pol | 10 µF | Panasonic ECS−H1CC106R |
| 18 | 3 | C38, C44, C51 | smd_cap_0402 | 100 nF | Yageo 04022F104Z7B20D |
| 19 | 3 | C39, C45, C52 | smd_cap_0402 | 33 nF | AVX 0402YD333KAT2A |
| 20 | 4 | C59−C61, C67 | smd_cap_0402 | 2.2 nF | AVX 0402YC223KAT2A |
| 21 | 3 | C69−C71 | smd_cap_0402 | 10 pF | Panasonic ECD−G0E100C |

| Item | QTY | Reference Designator | Footprint | Part | Part Number |
|---|---|---|---|---|---|
| 22 | 2 | C74 | smd_cap_1210 | 10 µF | Murata GRM32DR61E106KA12L |
| | | C77 | smd_cap_1210 | 10 µF | Murata GRM32DR61E106KA12L |
| 23 | 1 | C78 | smd_cap_0805 | NU | Panasonic ECP−U1C104MA5 |
| 24 | 3 | D1−D3 | smd_led_1206 | Amber | Lite−On LTST−C150AKT |
| 25 | 1 | D4 | smd_led_1206 | GREEN | Lite−On LTST−C150KGKT |
| 26 | 1 | FLT1 | ts−38s | TS−38S | Toyocom Filter |
| 27 | 7 | J1−J4, J6−J8 | sma_alt | SMA | Johnson Comp 142−0701−841 |
| 28 | 1 | J5 | jumper2 | HEADER 2 | |
| 29 | 9 | J9−J11, J13, J14, J16, J18, J22, J23 | sma_alt | NU_SMA | Johnson Comp 142−0701−841 |
| 30 | 4 | J12, J25, J26, J27 | hdr3_100ctr | HDR3 | Header 3 pos, 0.1 ctr |
| 31 | 2 | J17, J15 | smd_bridge_0402 | SMD3P_BRIDGE | Panasonic ERJ−2GE0R00X |
| 32 | 1 | J19 | jumper2 | HDR2 | Header 2 pos, 0.1 ctr |
| 33 | 2 | J21, J20 | smd_bridge_0402 | SMD3P_BRIDGE | Panasonic ERJ−2GE0R00X |
| 34 | 3 | J24, J28, J29 | jumper2 | HDR2 | Header 2 pos, 0.1 ctr |
| 35 | 1 | J30 | dcon25m | PARALLEL PORT | SPC Technology DB−25P−PCB |
| 36 | 1 | J31 | jumper4 | HDR4 | Header 4 pos, 0.1 ctr |
| 37 | 2 | J33, J32 | JUMPER3_SMD_WVIA_CDC7005 | HDR 3_cdc7005 | Use 0 W to short pins (see assy dwg) |
| 38 | 1 | J34 | jumper2 | HDR2 | Header 3 pos, 0.1 ctr |
| 39 | 1 | L1 | smd_cap_0603 | 75 Ω at100 MHz | Murata BLM18BA750SN1D |
| 40 | 1 | L2 | smd_cap_0603 | 470 nH | Murata LQW18ANR47J00D |
| 41 | 2 | L4, L3 | smd_cap_0603 | 180 nH | Panasonic ELJ−FJR18JF2 |
| 42 | 3 | L5−L7 | smd_cap_0603 | 75 Ω at 100 MHz | Murata BLM18BA750SN1D |
| 43 | 1 | L8 | smd_cap_0805 | 2.2 nH | J W Miller Magnetics PM0805−2N2M |
| 44 | 1 | P1 | banana_jack | PWR_IN | SPC Technologies 845R |
| 45 | 1 | P2 | banana_jack | GND | SPC Technologies 845B |
| 46 | 18 | R1, R2, R7, R9, R10, R11, R16, R18−R20, R22, R24, R26, R27, R30, R35, R48, R50 | smd_res_0402 | NU 100 Ω | Panasonic ERJ−2RKF1000X |
| 47 | 2 | R3, R12 | smd_res_0402 | NU | Panasonic ERJ−2GEJ510X |

| Item | QTY | Reference Designator | Footprint | Part | Part Number |
|---|---|---|---|---|---|
| 48 | 7 | R4, R6, R13, R15, R62, R63, R65 | smd_res_0402 | 100 Ω | Panasonic ERJ−2RKF1000X |
| 49 | 6 | R5, R8, R14, R17, R21, R23 | smd_res_0402 | 150 Ω | Panasonic ERJ−2RKF1500X |
| 50 | 10 | R25, R57, R59, R60, R68−R71, R74, R75 | smd_res_0402 | 10 kΩ | Panasonic ERJ−2RKF1002X |
| 51 | 2 | R28, R45 | smd_res_0402 | NU 0 Ω | Panasonic ERJ−2GE0R00X |
| 52 | 4 | R29, R32, R49, R80 | smd_res_0402 | NU 150 Ω | Panasonic ERJ−2RKF1500X |
| 53 | 2 | R38, R31 | smd_res_0402 | 130 Ω | Panasonic ERJ−2GEJ131X |
| 54 | 10 | R33, R34, R41, R42, R82,−R87 | smd_res_0402 | 0 Ω | Panasonic ERJ−2GE0R00X |
| 55 | 2 | R43, R36 | smd_res_0402 | 82 Ω | Panasonic ERJ−2GEJ820X |
| 56 | 2 | R37, R44 | smd_res_0402 | NU | NU |
| 57 | 2 | R39, R40 | smd_res_0402 | 62 W | Panasonic ERJ−2GEJ620X |
| 58 | 2 | R47, R46 | smd_res_0402 | NU 100 | Panasonic ERJ−2RKF1000X |
| 59 | 4 | R51, R64, R66, R67 | smd_res_0402 | 100 kΩ | Panasonic ERJ−2RKF1003X |
| 60 | 1 | R52 | smd_res_0402 | 160 Ω | Panasonic ERJ−2RKF1002X |
| 61 | 2 | R53, R72 | smd_res_0402 | 4.7 kΩ | Panasonic ERJ−2RKF1472X |
| 62 | 3 | R54−R56 | smd_res_0402 | 750 | Panasonic ERJ−2GEJ131X |
| 63 | 1 | R58 | smd_res_0402 | NU 12K 1% | Panasonic ERJ−2RKF4121X |
| 64 | 1 | R61 | smd_cap_0402 | 1.5 kΩ | Panasonic ERJ−2RKF1501X |
| 65 | 1 | R73 | smd_res_0402 | 180 Ω | Panasonic ERJ−2RKF1472X |
| 66 | 3 | R78, R79, R81 | smd_res_0402 | 22 Ω | Panasonic ERJ−2GEJ220X |
| 67 | 2 | SW2, SW1 | switch_reset | SW PUSHBUTTON | KT11P3JM |
| 68 | 2 | TP1, TP2 | testpin_30dia | T POINT R | Test point |
| 69 | 1 | U2 | mbga_pt8mm_64_skt | CDCM7005 | Texas Instruments CDCM7005 |
| 70 | 1 | U3 | soic14 | SN74LV125 | Texas Instruments SN74LV125AD |
| 71 | 1 | U4 | soic_round_4 | NU SGA−4586 | NU Sirenza SGA−4586 |
| 72 | 1 | U5 | soic8 | OPA341 | Texas Instruments OPA341UA |
| 73 | 1 | VCXO1 | VCXO_6 | VCXO_6 | Toyocom VCXO |
| 74 | 4 | MP3 | STAND OFF | | Legs for PCB |
| 75 | 4 | MP2 | SCREW | | Legs for PCB |

## 6.2 Board Layout

*Figure 6−1. Component View and Silkscreen (Top View)*

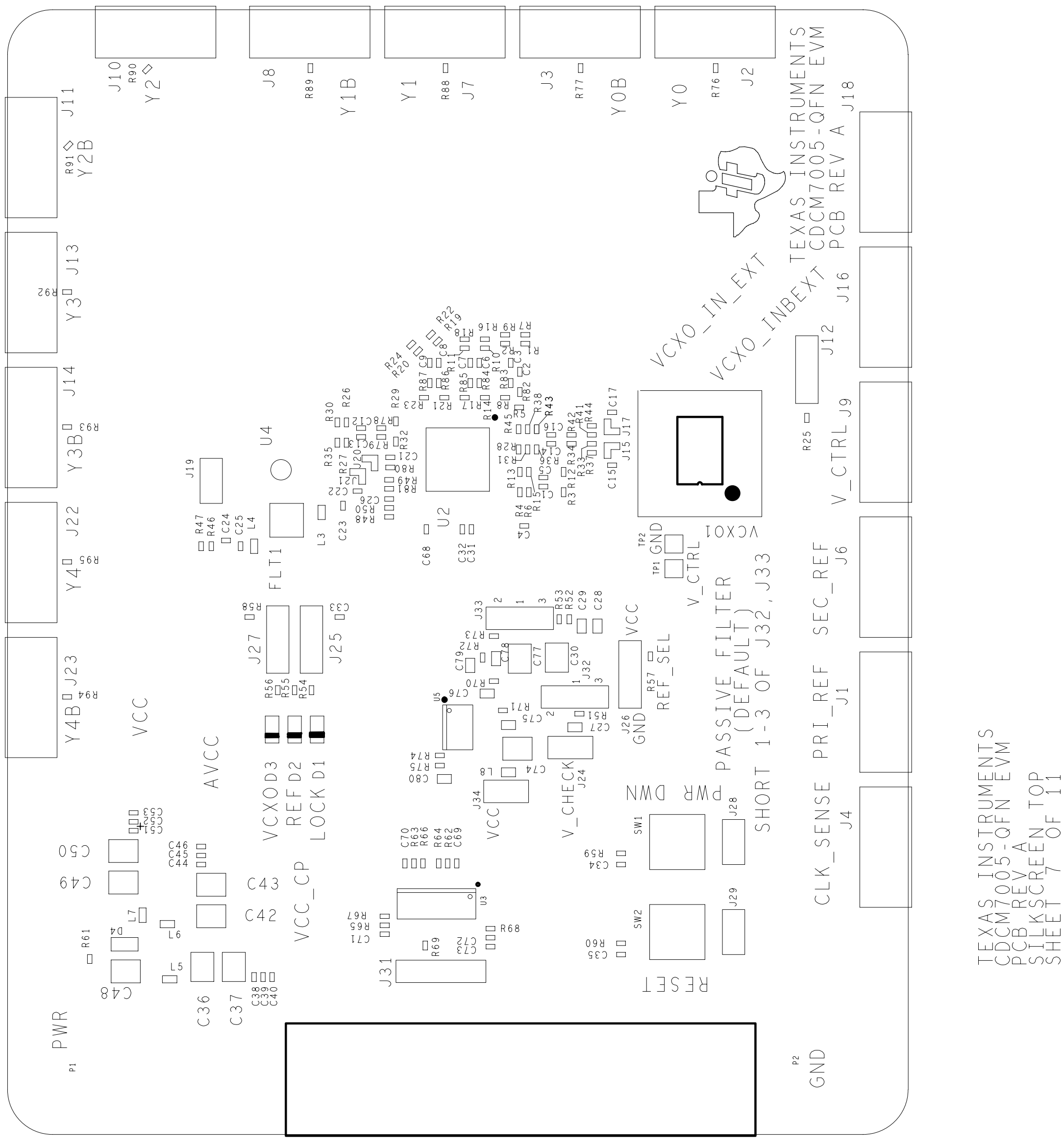


*Figure 6−2. Component View and Silkscreen (Bottom View)*

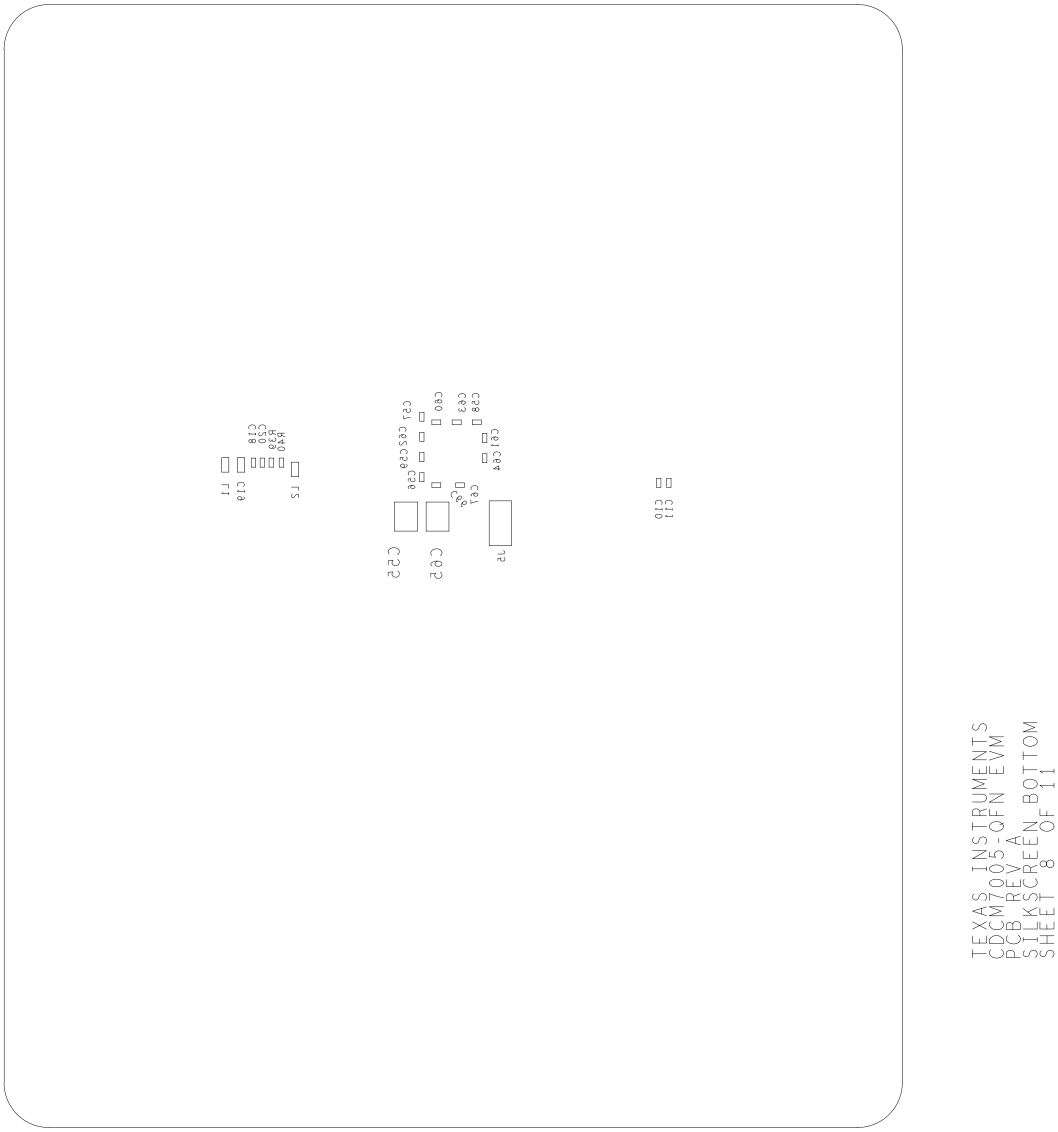


*Figure 6−3. Top Layer View*

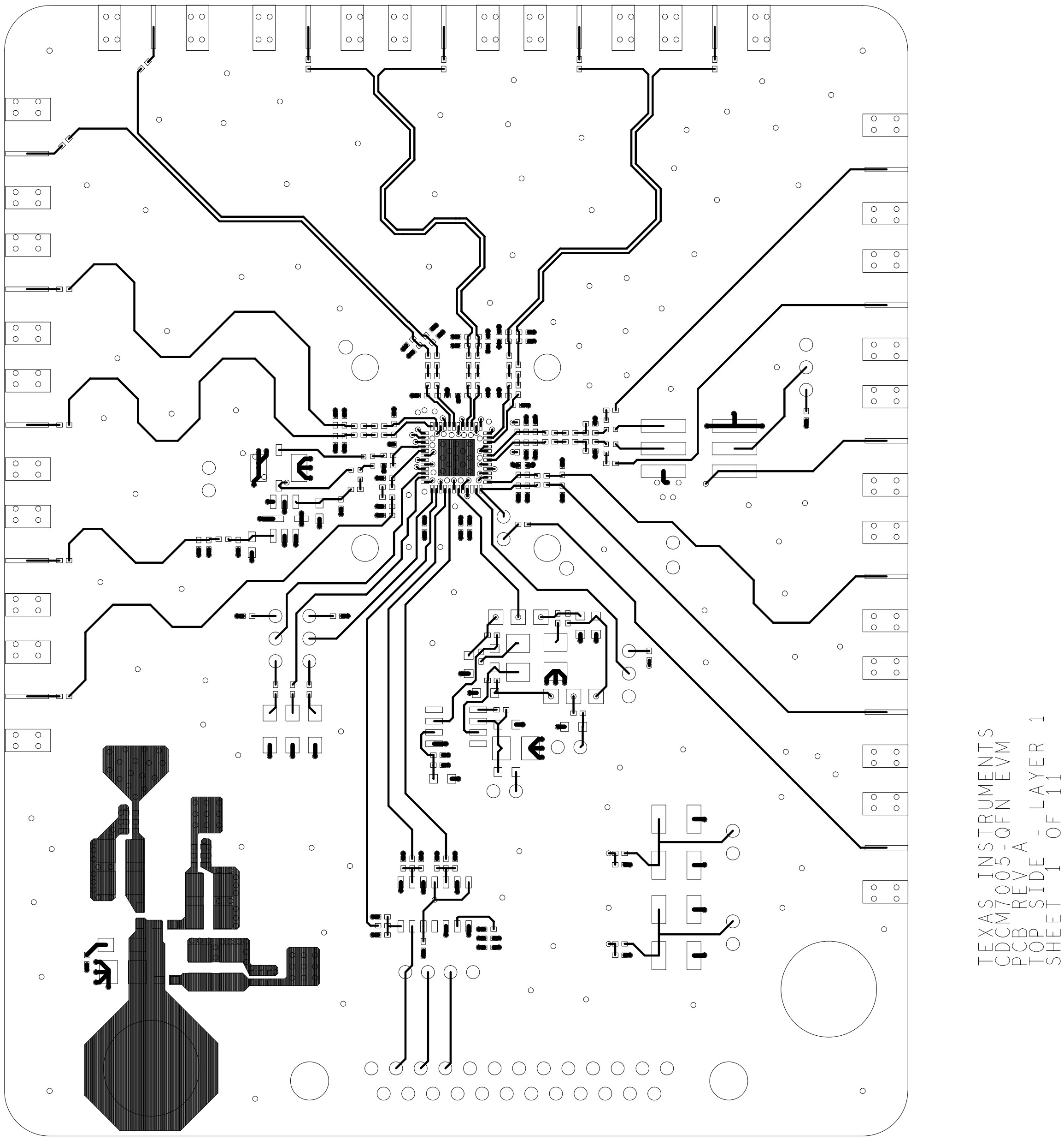


*Figure 6−4. Bottom Layer View*

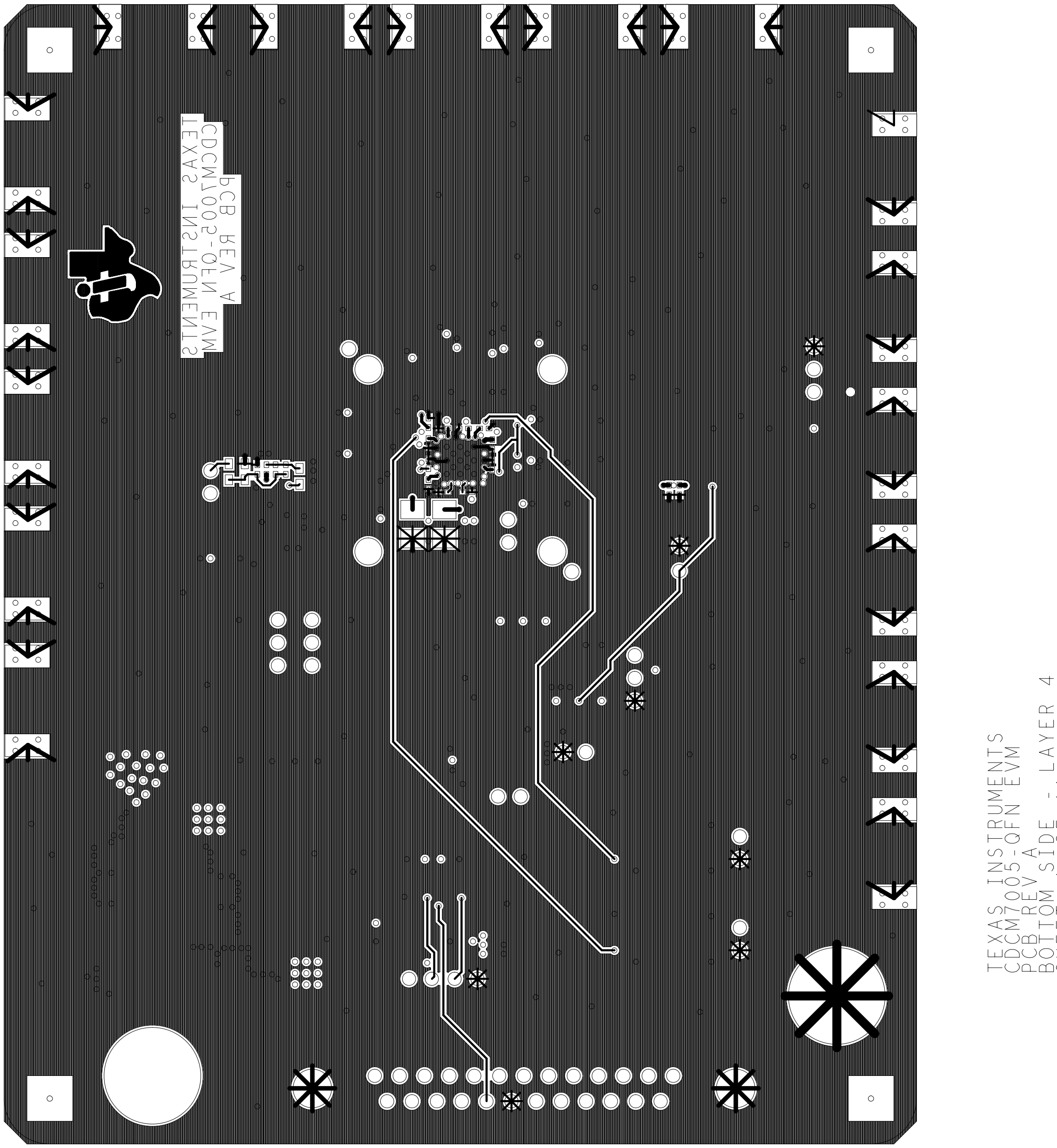


*Figure 6−5. Ground Plane View*

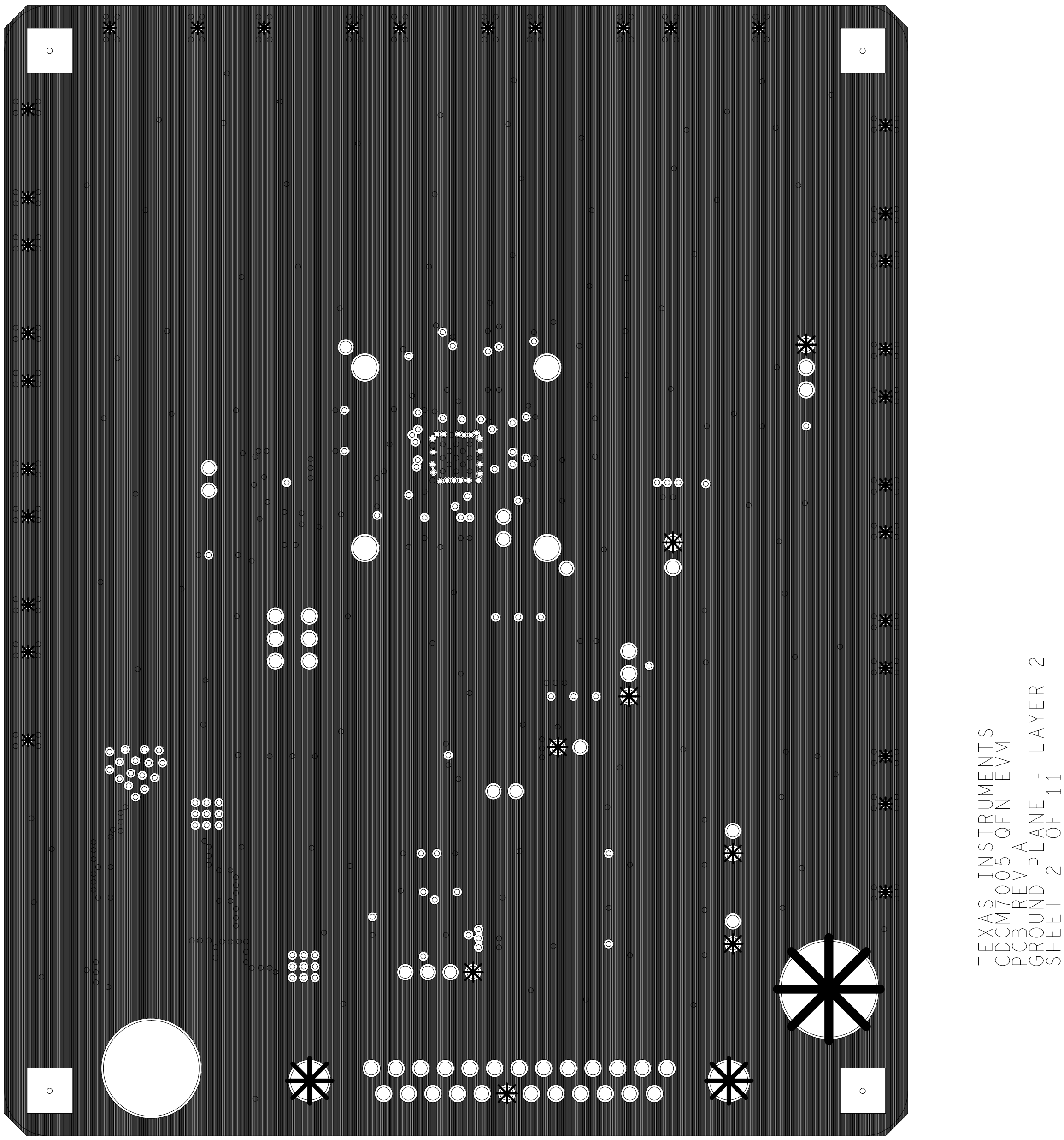
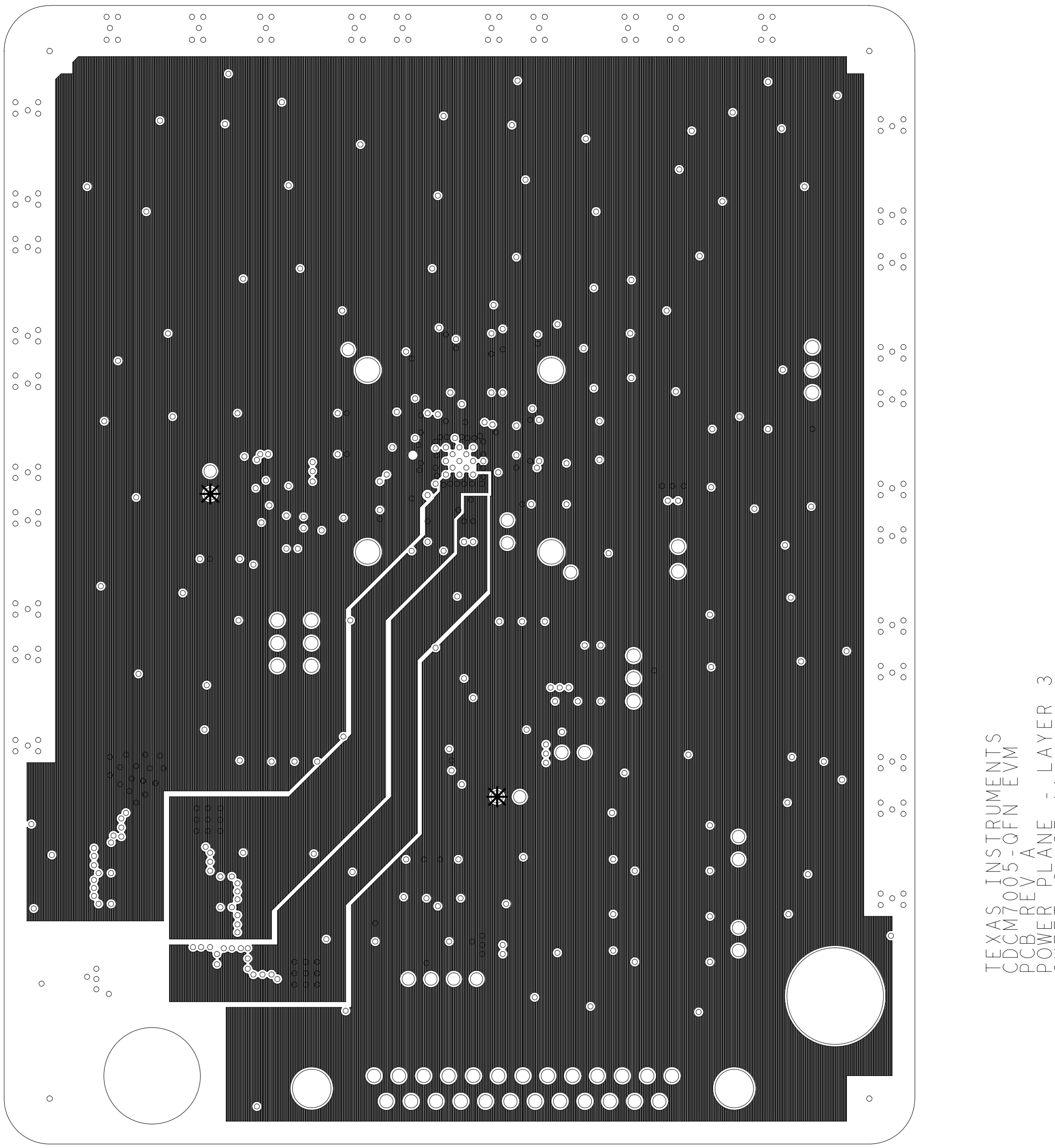
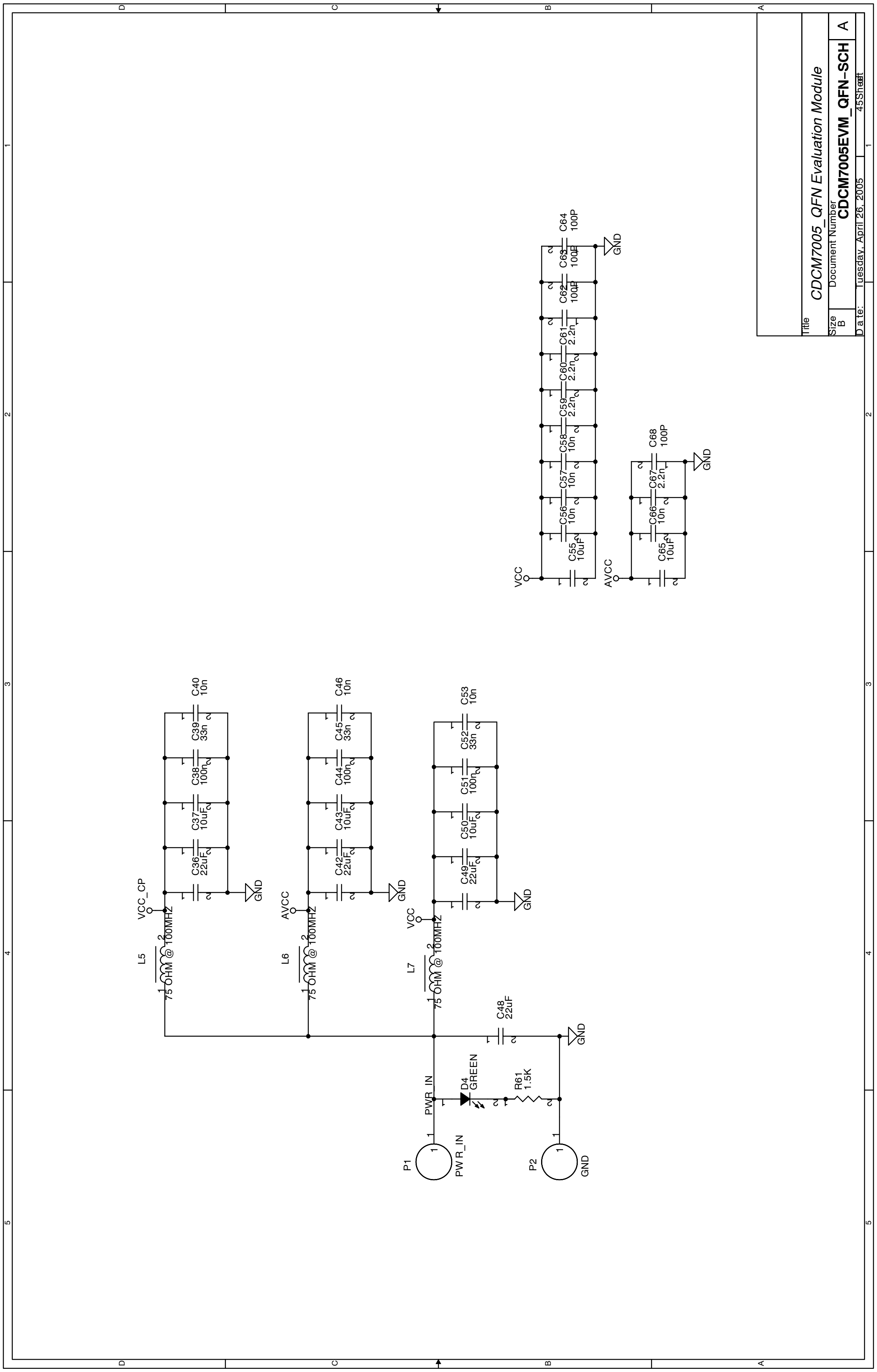


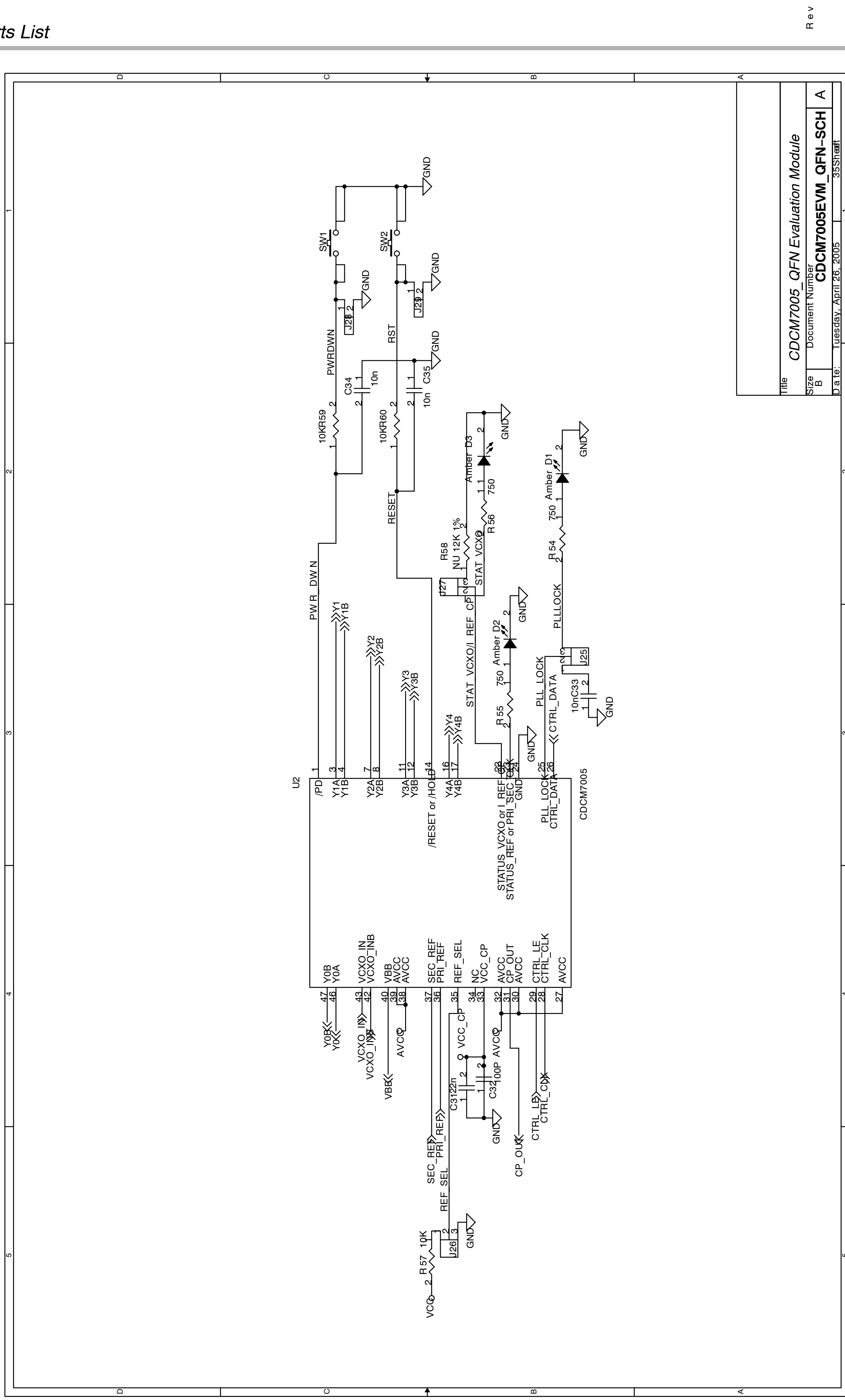
*Figure 6−6. Power Layer View*

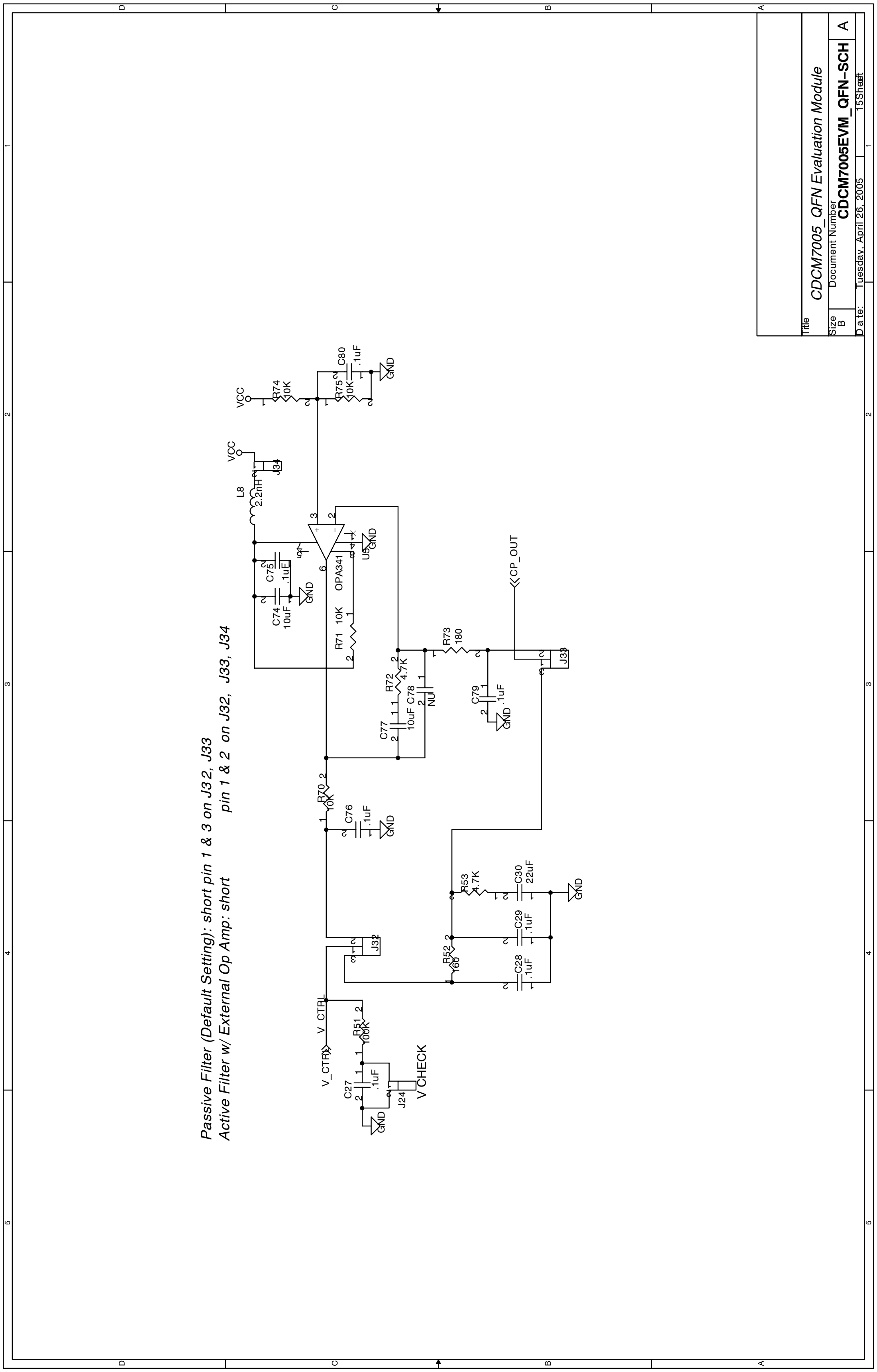


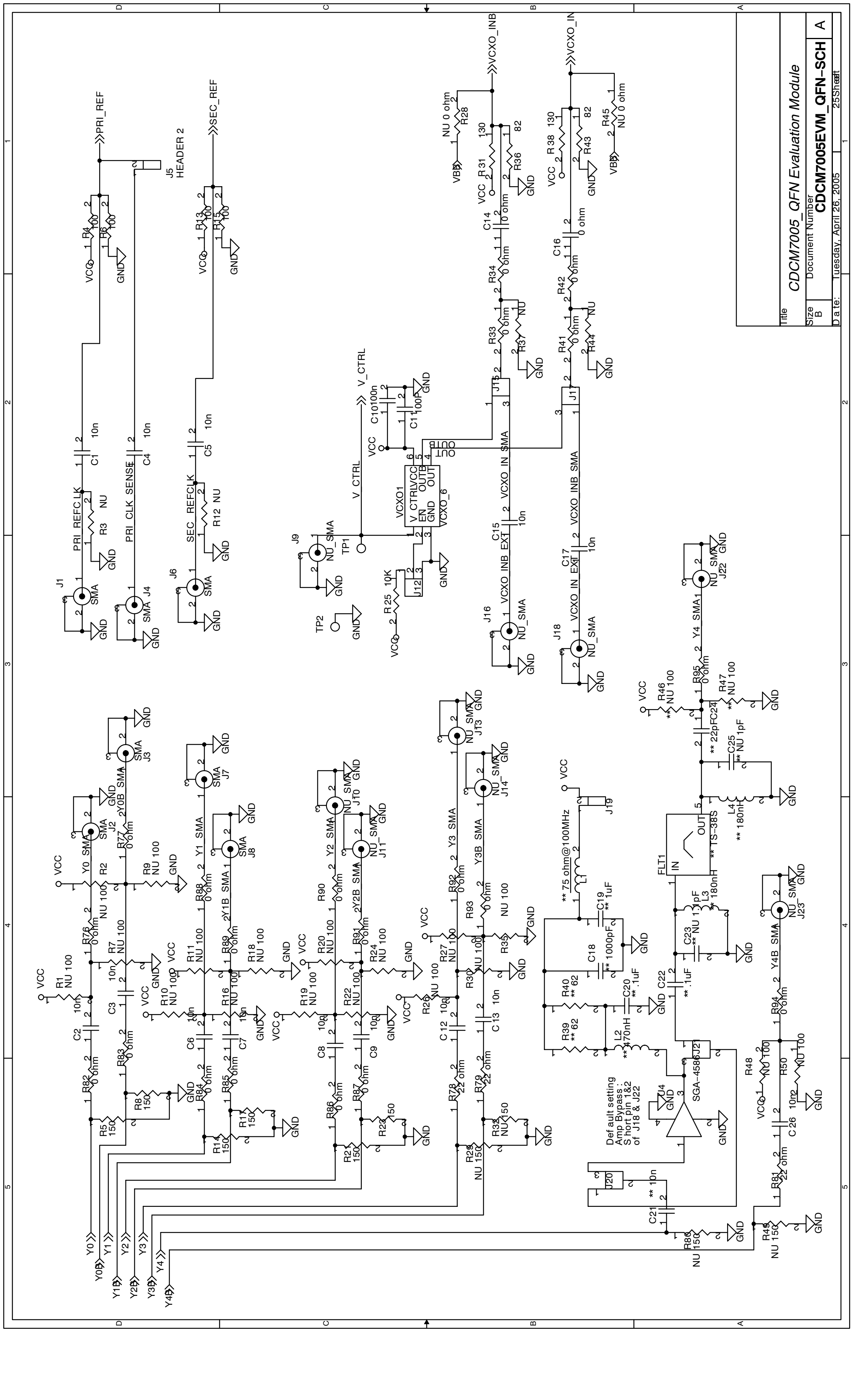

## 6.3 Schematics

The following pages contain the schematics for the CDCM7005 (QFN package).

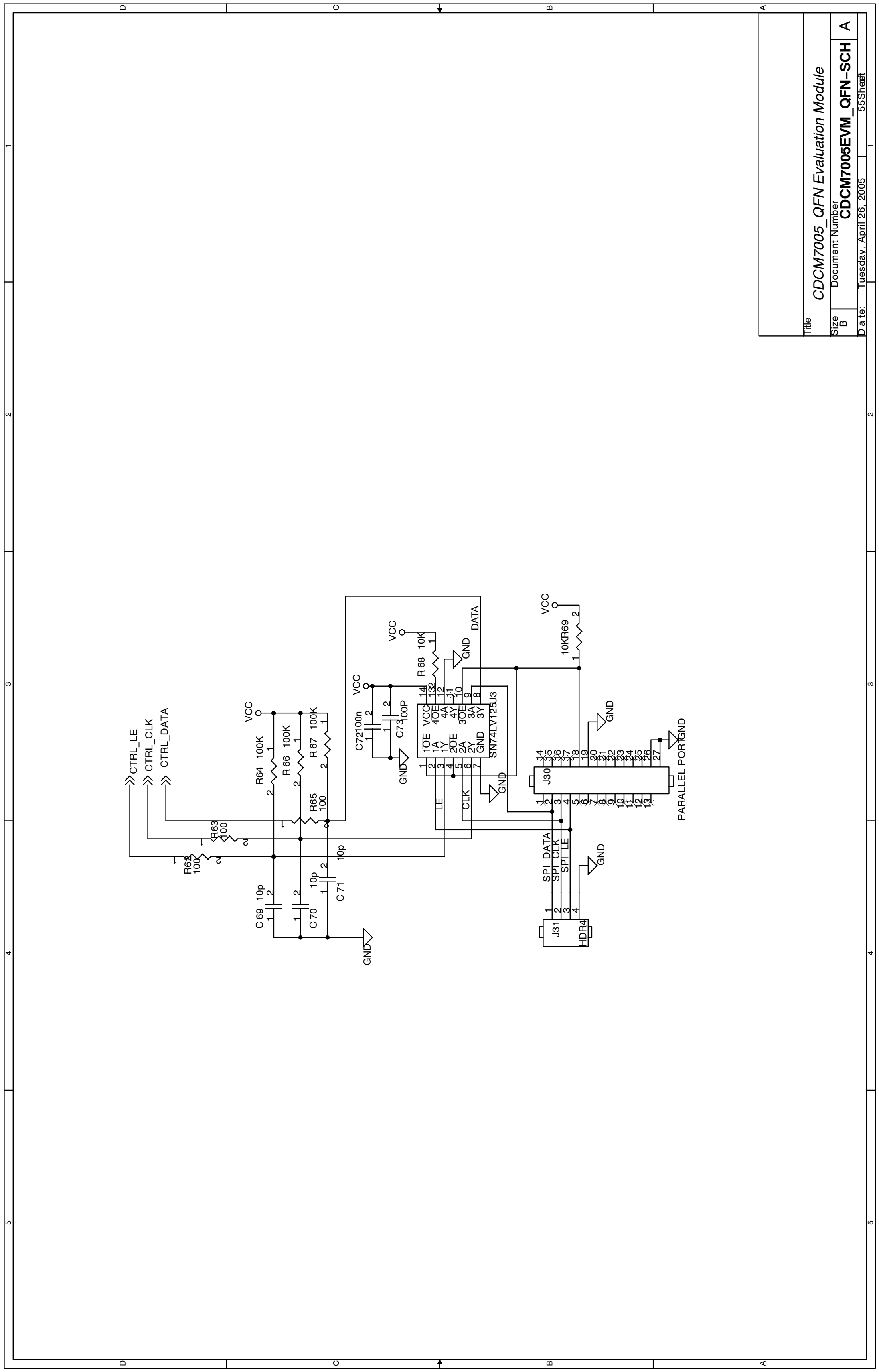

CDCM7005_QFN Evaluation Module
Title
Size
B
Document Number
CDCM7005EVM_QFN-SCH
Rev
A
Date: Tuesday, April 26, 2005
Sheet 4 of 5
VCC_CP
AVCC
VCC
GND
L5
L6
L7
75 OHM @ 100MHZ
C36 22uF
C37 10uF
C38 100n
C39 33n
C40 10n
C42 22uF
C43 10uF
C44 100n
C45 33n
C46 10n
C49 22uF
C50 10uF
C51 100n
C52 33n
C53 10n
C48 22uF
D4 GREEN
R61 1.5K
PWR_IN
P1
P2
C55 10uF
C56 10n
C57 10n
C58 10n
C59 2.2n
C60 2.2n
C61 2.2n
C62 100P
C63 100P
C64 100P
C65 10uF
C66 10n
C67 2.2n
C68 100P


Rev
Title
CDCM7005_QFN Evaluation Module
Size
B
Document Number
CDCM7005EVM_QFN-SCH
A
Date: Tuesday, April 26, 2005
U2
CDCM7005


CDCM7005_QFN Evaluation Module
Document Number
CDCM7005EVM_QFN-SCH
Rev
A
Size
B
Date: Tuesday, April 26, 2005
Passive Filter (Default Setting): short pin 1 & 3 on J32, J33
Active Filter w/ External Op Amp: short pin 1 & 2 on J32, J33, J34
VCC
R74
10K
R75
10K
C80
.1uF
GND
L8
2.2nH
J34
OPA341
U5
C75
.1uF
C74
10uF
R71 10K
R72
4.7K
C77
10uF
C78
NU
R73
180
C79
.1uF
CP_OUT
J33
R70
10K
C76
.1uF
J32
R53
4.7K
C30
22uF
C29
.1uF
R52
180
C28
.1uF
V_CTRL
R51
100K
C27
.1uF
J24
V CHECK



Rev
Title
CDCM7005_QFN Evaluation Module
Size
B
Document Number
CDCM7005EVM_QFN-SCH
A
Date: Tuesday, April 26, 2005


Title
CDCM7005_QFN Evaluation Module
Size
B
Document Number
CDCM7005EVM_QFN-SCH
Rev
A
Date: Tuesday, April 26, 2005
Sheet 5 of 5
CTRL_LE
CTRL_CLK
CTRL_DATA
VCC
GND
R64 100K
R66 100K
R67 100K
R65 100
R68 10K
10K R69
C69 10p
C70 10p
C71 10p
C72 100n
C73 100P
SN74LV125
U3
J30
PARALLEL PORT
J31
HDR4
SPI_DATA
SPI_CLK
SPI_LE
DATA
LE
CLK